

## **CLAIMS**

What is claimed is:

- 1 1. A memory cell comprising:
  - 2 a first PMOS transistor;
  - 3 a first NMOS transistor coupled to the first PMOS transistor;
  - 4 a second PMOS transistor; and
  - 5 a second NMOS transistor coupled to the second PMOS transistor;
  - 6 the first and second PMOS transistors receiving a bias control signal.
- 1 2. The memory cell of claim 1 further comprising:
  - 2 a first storage node coupled between the first PMOS transistor and the
  - 3 first NMOS transistor; and
  - 4 a second storage node coupled between the second PMOS transistor and
  - 5 the second NMOS transistor.
- 1 3. The memory cell of claim 2 wherein the bias control signal delivers a  
2 forward bias voltage to the first and second PMOS transistors whenever the  
3 memory cell is operating in a standby mode.
- 1 4. The memory cell of claim 3 wherein the forward bias voltage enables the  
2 first storage node to maintain a storage value by providing an off-state leakage  
3 current from the first PMOS transistor.
- 1 5. The memory cell of claim 2 wherein the bias control signal delivers a  
2 reverse bias voltage to the first and second PMOS transistors whenever the  
3 memory cell is operating in a read mode.

1       6.     The memory cell of claim 5 wherein the reverse bias voltage prevents the  
2     memory cell from switching its value during the read mode.

1       7.     A memory device comprising:  
2              an N-well;  
3              a plurality of memory cells, each memory cell including:  
4                  a P-channel component; and  
5                  a N-channel component, the P-channel component being formed  
6                  within the N-well;  
7                  a gap cell formed within the N-well; and  
8                  a contact within the gap cell that provides a bias control signal to each of  
9                  the P-channel components within a memory cell.

1       8.     The memory device of claim 7 wherein the P-channel component of each  
2     memory cell comprises:  
3              a first PMOS transistor; and  
4              a second PMOS transistor, the first and second PMOS transistors receiving  
5              a bias control signal.

1       9.     The memory device of claim 8 wherein the N-channel component of each  
2     memory cell comprises:  
3              a first NMOS transistor coupled to the first PMOS transistor; and  
4              a second NMOS transistor coupled to the second PMOS transistor;

1       10.    The memory device of claim 9 further comprising:  
2              a first storage node coupled between the first PMOS transistor and the  
3     first NMOS transistor; and  
4              a second storage node coupled between the second PMOS transistor and

5 the second NMOS transistor.

1 11. The memory device of claim 10 wherein the bias control signal delivers a  
2 forward bias voltage to the first and second PMOS transistors whenever the  
3 memory cell is operating in a standby mode.

1 12. The memory device of claim 11 wherein the forward bias voltage enables  
2 the first storage node to maintain a storage value by providing an off-state  
3 leakage current from the first PMOS transistor.

1 13. The memory device of claim 10 wherein the bias control signal delivers a  
2 reverse bias voltage to the first and second PMOS transistors whenever the  
3 memory cell is operating in a read mode.

1 14. The memory device of claim 13 wherein the reverse bias voltage prevents  
2 the memory cell from switching its value during the read mode.

1 15. A computer system comprising:

2 a microprocessor; and

3 a cache memory device, the cache memory device including:

4 a plurality of memory cells, each memory cell including a P-  
5 channel component and a N-channel component, the P-channel  
6 component formed within the N-well;

7 a gap cell formed within the N-well; and

8 a contact within the gap cell that provides a bias control signal to  
9 each of the P-channel components within a memory cell.

1 16. The computer system of claim 15 wherein the P-channel component of  
2 each memory cell comprises:

3 a first PMOS transistor; and

4           a second PMOS transistor, the first and second PMOS transistors receiving  
5    a bias control signal.

1    17.   The computer system of claim 16 wherein the N-channel component of  
2    each memory cell comprises:

3           a first NMOS transistor coupled to the first PMOS transistor; and  
4           a second NMOS transistor coupled to the second PMOS transistor;

1    18.   The computer system of claim 17 further comprising:

2           a first storage node coupled between the first PMOS transistor and the  
3    first NMOS transistor; and  
4           a second storage node coupled between the second PMOS transistor and  
5    the second NMOS transistor.

1    19.   The computer system of claim 18 wherein the bias control signal delivers a  
2    forward bias voltage to the first and second PMOS transistors whenever the  
3    memory cell is operating in a standby mode.

1    20.   The computer system of claim 19 wherein the forward bias voltage  
2    enables the first storage node to maintain a storage value by providing an off-  
3    state leakage current from the first PMOS transistor.

1    21.   The computer system of claim 18 wherein the bias control signal delivers a  
2    reverse bias voltage to the first and second PMOS transistors whenever the  
3    memory cell is operating in a read mode.

1    22.   The computer system of claim 21 wherein the reverse bias voltage  
2    prevents the memory cell from switching its value during the read mode.

1    23.   The computer system of claim 15 wherein the cache memory device is

2 coupled to the microprocessor.

1 24. The computer system of claim 15 wherein the cache memory device is  
2 included within the microprocessor.